CLAIMS

1. A non-volatile semiconductor memory device, comprising:

a plurality of bit lines;

a plurality of word lines; and

a plurality of dual cell storage elements, each of said dual cell storage elements including at least a source device, a drain device and a select device,

wherein two out of a total of six of said source devices and said drain devices in three adjacent dual cell memory units along a particular one of said word lines are able to be programmed or read simultaneously.

2. A non-volatile semiconductor memory device as recited in claim 1,

wherein each of said select devices couples to one of said word lines, and

wherein each of said source devices and said drain devices couple between one of said bit lines and one of said select devices.

3. A non-volatile semiconductor memory device as recited in claim 1,

wherein each of said source device and said drain devices include a floating gate.

4. A non-volatile semiconductor memory device as recited in claim 3, wherein said select devices do not include a floating gate.

5. A non-volatile semiconductor memory device as recited in claim 1, wherein said storage elements are Flash type storage elements.

6. A non-volatile semiconductor memory device as recited in claim 1, wherein said storage elements are EEPROM type storage elements.

7. A non-volatile semiconductor memory device as recited in claim 1, wherein said non-volatile semiconductor memory device is provided within a memory card.

8. A portable memory card, comprising:

a data storage array, said data storage array including at least a plurality of bit lines, a plurality of word lines, and a plurality of dual cell storage elements, each of said dual cell storage elements including at least a source device, a drain device and a select device; and

a controller operatively connected to said storage elements, said controller operating to control reading and writing to said data storage array,

wherein two of said source devices and said drain devices in three adjacent dual cell storage elements along a particular one of said word lines are able to be programmed or read simultaneously.

9. A portable memory card as recited in claim 8,

wherein each of said select devices couple to one of said word lines,

wherein each of said source devices and said drain devices couple between one of said bit lines and one of said select devices, and

wherein the three adjacent dual cell storage elements together include three of said source devices and three of said drain devices.

10. A portable memory card as recited in claim 8, wherein said data storage array is provided on a single semiconductor chip.

11. A portable memory card as recited in claim 8, wherein said portable memory card is a memory system on a chip.

12. A method for reading data from a non-volatile memory, said method comprising:

identifying three adjacent memory elements along a particular word line, each of the three adjacent memory elements being coupled between an adjacent pair of bit lines, each of the three adjacent memory elements including at least a pair of memory cells;

coupling one of the bit lines in each of the adjacent pairs of the bit lines surrounding each of two of the three adjacent memory elements having a memory cell to be read to a low potential;

coupling a read voltage to the memory cell to be read in each of two of the three adjacent memory elements having a memory cell to be read;

coupling an overdrive voltage to the other memory cells in the three adjacent memory cells; and

thereafter simultaneously reading data from one of the two memory cells in the two of the three adjacent memory elements having a memory cell to be read via another of the bit lines in each of the adjacent pairs of the bit lines surrounding each of two of the three adjacent memory elements having a memory cell to be read.

13. A method as recited in claim 12, wherein said reading comprises:

coupling the another of the bit lines in each of the adjacent pairs of the bit lines surrounding each of two of the three adjacent memory elements having a memory cell to be read to sense amplifiers, respectively; and

simultaneously reading data from one of the two memory cells in the two of the three adjacent memory elements having a memory cell to be read using the sense amplifiers.

14. A method as recited in claim 12, wherein each of the three adjacent memory elements further including at least a select element.

15. A method as recited in claim 14, wherein said method further comprises:

operating the select element in the one of the three adjacent memory elements not having a memory cell to be read to isolate the two of the three adjacent memory elements having a memory cell to be read from one another.

16. A method as recited in claim 15, wherein said operating provides a positive voltage on those of the bit lines that are not coupled to the low potential.

17. A method as recited in claim 15, wherein said operating comprises coupling another of the bit lines in each of the adjacent pairs of the bit lines surrounding each of two of the three adjacent memory elements having a memory cell to be read to a potential that enables the select element to become non-conductive.

18. A method as recited in claim 15, wherein said operating of the select element is controlled based in part on the particular word line.

19. A method as recited in claim 15, wherein the low potential is ground.

20. A method for reading data from a non-volatile memory, said method comprising:

providing a non-volatile memory having an array of memory elements, a plurality of bit lines, a plurality of word lines, and a plurality of gate control signals;

identifying first, second and third memory elements that are adjacent one another along a particular word line, each of the first, second and third memory elements including at least a pair of memory cells and a select gate;

identifying first, second, third and fourth bit lines that are adjacent one another along the particular word line, the first memory element being interposed between the first bit line and the second bit line, the second memory element being interposed

between the second bit line and the third bit line, and the third memory element being interposed between the third bit line and the fourth bit line;

identifying a first memory cell in the first memory element and a second memory element in the third memory element to be read;

coupling the first bit line and the fourth bit line to a low potential;

coupling the other memory cells in the first, second and third memory elements other than the first and second memory cells to a high potential;

coupling the particular word line to the select gates for the each of the first, second and third memory elements;

coupling a read voltage to the first and second memory cells to be read; and

thereafter simultaneously reading data from one of the first and second memory cells via the second and third bit lines.

21. A method as recited in claim 20, wherein the memory cells are floating gate memory cells.

22. A method as recited in claim 20, wherein the low potential is ground potential.

23. A method as recited in claim 20, wherein the high potential is an overdrive voltage.

24. A method for programming data to a non-volatile memory, said method comprising:

identifying three adjacent memory elements along a particular word line, each of the three adjacent memory elements being coupled between an adjacent pair of bit lines, each of the three adjacent memory elements including at least a pair of memory cells;

coupling one of the bit lines in each of the adjacent pairs of the bit lines surrounding each of two of the three adjacent memory elements having a memory cell to be programmed to a program level potential;

coupling the other of the bit lines in each of the adjacent pairs of the bit lines surrounding each of two of the three adjacent memory elements having a memory cell to be programmed to a low potential;

coupling a program gate voltage to the memory cell to be programmed in each of two of the three adjacent memory elements having a memory cell to be read;

coupling an overdrive voltage to the other memory cells in the three adjacent memory cells; and

thereafter simultaneously programming data to one of the two memory cells in the two of the three adjacent memory elements having a memory cell to be programmed.

25. A method as recited in claim 24, wherein the low potential is a ground potential.

26. A method as recited in claim 24, wherein each of the three adjacent memory elements further including at least a select element.

27. A method as recited in claim 26, wherein said method further comprises:

operating the select element in a fourth adjacent memory element not having a memory cell to be programmed to isolate the fourth adjacent memory element from being programmed.

28. A method as recited in claim 27, wherein said operating of the select element is controlled based in part on the particular word line.

29. A method as recited in claim 27, wherein the low potential is ground.

30. A method for programming data to a non-volatile memory, said method comprising:

providing a non-volatile memory having an array of memory elements, a plurality of bit lines, a plurality of word lines, and a plurality of gate control signals;

identifying first, second and third memory elements that are adjacent one another along a particular word line, each of the first, second and third memory elements including at least a pair of memory cells and a select gate;

identifying first, second, third and fourth bit lines that are adjacent one another along the particular word line, the first memory element being interposed between the first bit line and the second bit line, the second memory element being interposed between the second bit line and the third bit line, and the third memory element being interposed between the third bit line and the fourth bit line;

identifying a first memory cell in the first memory element and a second memory element in the third memory element to be programmed;

coupling the first bit line and the fourth bit line to a program level potential;

coupling the other memory cells in the first, second and third memory elements other than the first and second memory cells to a high potential;

coupling the particular word line to the select gates for the each of the first, second and third memory elements;

coupling a program voltage to the first and second memory cells to be programmed; and

thereafter simultaneously programming data to the first and second memory cells.

31. A method as recited in claim 30, wherein the memory cells are floating gate memory cells.

32. A method as recited in claim 30, wherein the low potential is ground potential.

33. A method as recited in claim 30, wherein the high potential is an overdrive voltage.